semi

A Paradigm shift through panel level processing

Garry Pycroft

VP Sales & Marketing – Deca Technologies

3D & SYSTEMS SUMMIT

28-30 JAN 2019

Deca Technologies

Definition of “Paradigm Shift“

Merriam-Webster states :

an important change that happens when the usual way of thinking about or doing something is replaced by a new and different way

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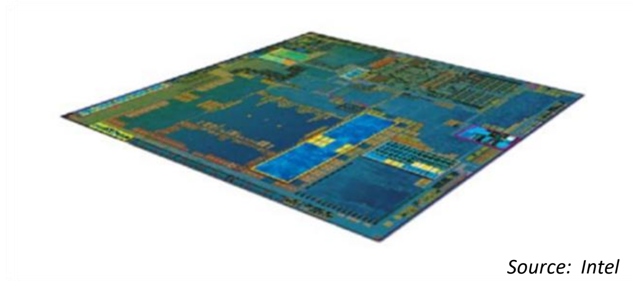
- **A means to provide new capabilities of value to the industry within a short horizon**
- **A means to enable a more cost effective solution to the industry's needs**
- **Where both are being provided then this must surely be “An important change”**

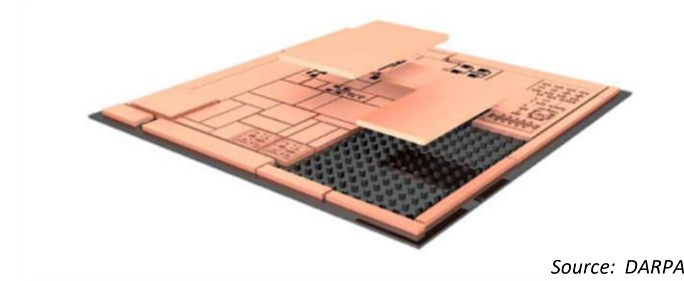
Industry Direction

Today – Monolithic SoCs



Source: Intel

Tomorrow – Heterogeneous SoCs



Source: DARPA

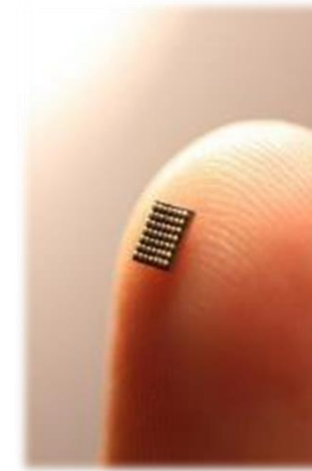
Heterogeneous SoC:

A high performance SiP based on 2.5D or 3D interconnect

Created through integration of chiplets vs. monolithically

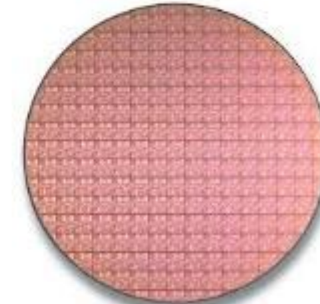
Using standardized, high bandwidth, low power, low latency interfaces

Deca Technologies Overview



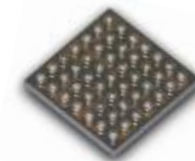
- Advanced wafer level electronic interconnect foundry
- Providing WLCSP turnkey services on 200 & 300mm wafers
- Private company – fully diluted ownership
  - Cypress Semiconductor 49%
  - ASE 21%
  - Large customer 18%
  - SunPower 2%
  - Employees 10%
- Shipping WLCSP in high volume to all leading handset OEM's
  - > 80% of our business is in mobile market
- Introduced M-Series FOWLP

Our Heritage - Solar to Semiconductors



SUNPOWER

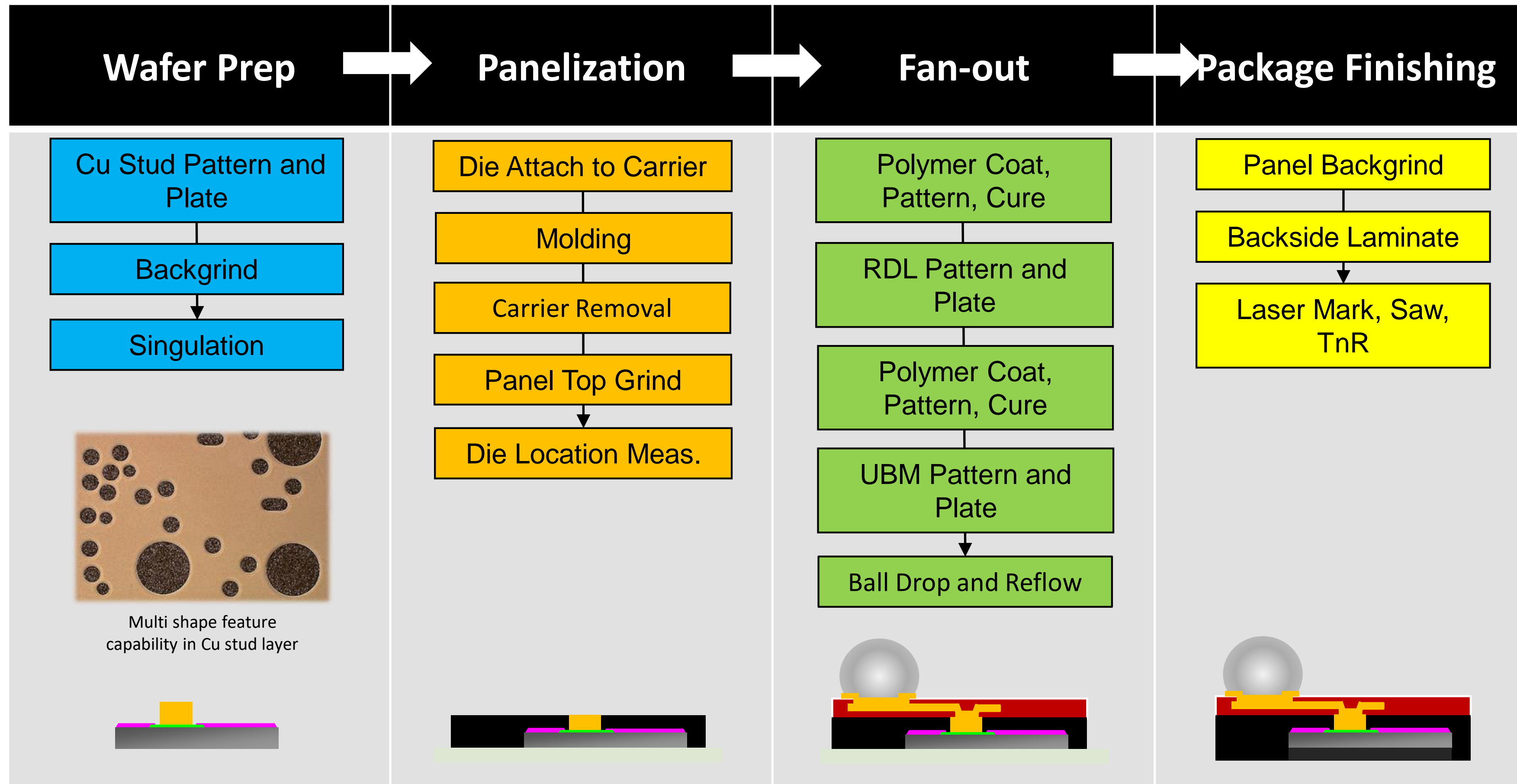
Deca Technologies



WLCSP

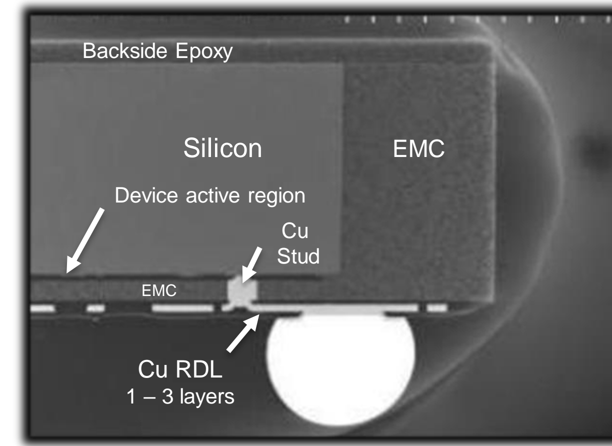
Fan-Out

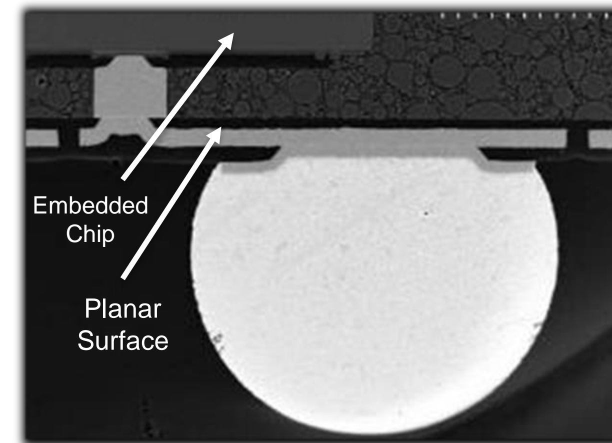
M-Series Basic Process Flow



M-Series™ Fan-out Technology

- Chips-first, chips-up fan-out technology with fully encapsulated active region
- Planar patterning surface: 5µm line & space with 2µm line & space in development
- Adaptive patterning to enable high yields in scaling to advanced silicon with tight IO pitch
- Excellent board level reliability with silicon protected by molded stress buffer
- Unique structure enables low fan-out ratios with excellent manufacturability
- Full opaque encapsulation for light sensitive devices

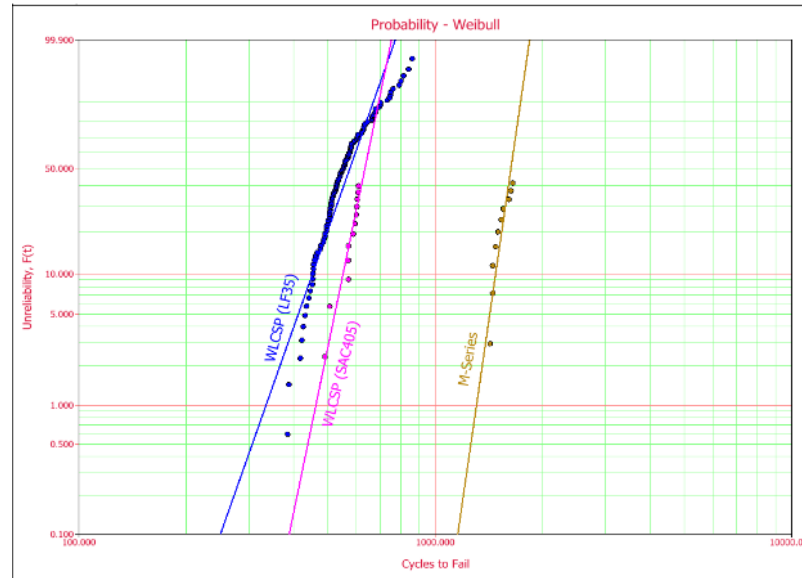




Only Deca's M-Series™ & TSMC's InFO™ provide advanced face-up fan-out technology

M-Series Breakthrough BLR

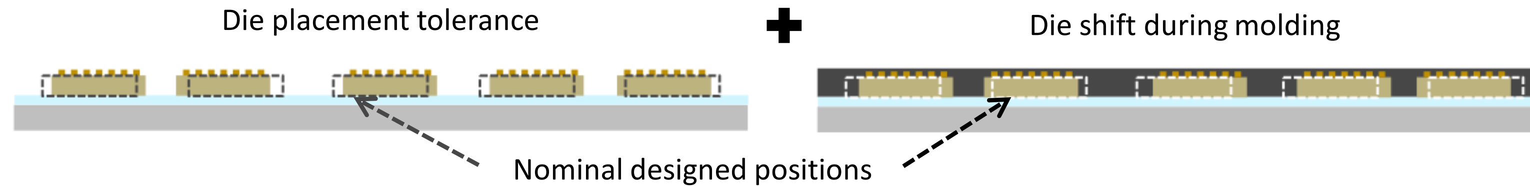
- M-Series outperforms standard WLCSP by over 250%

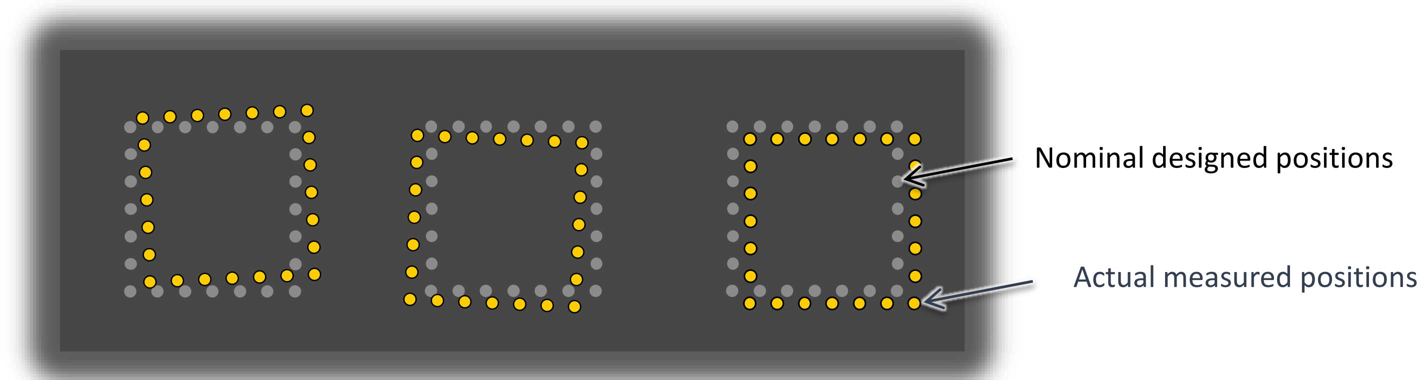


6x6 mm die in WLCSP and in 6.25 x 6.25mm package, 0.5mm thick
Board level temperature cycle on JEDEC 1mm board, SAC 405

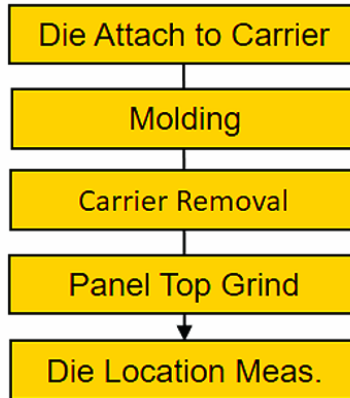
Die shift - #1 challenge in fan-out

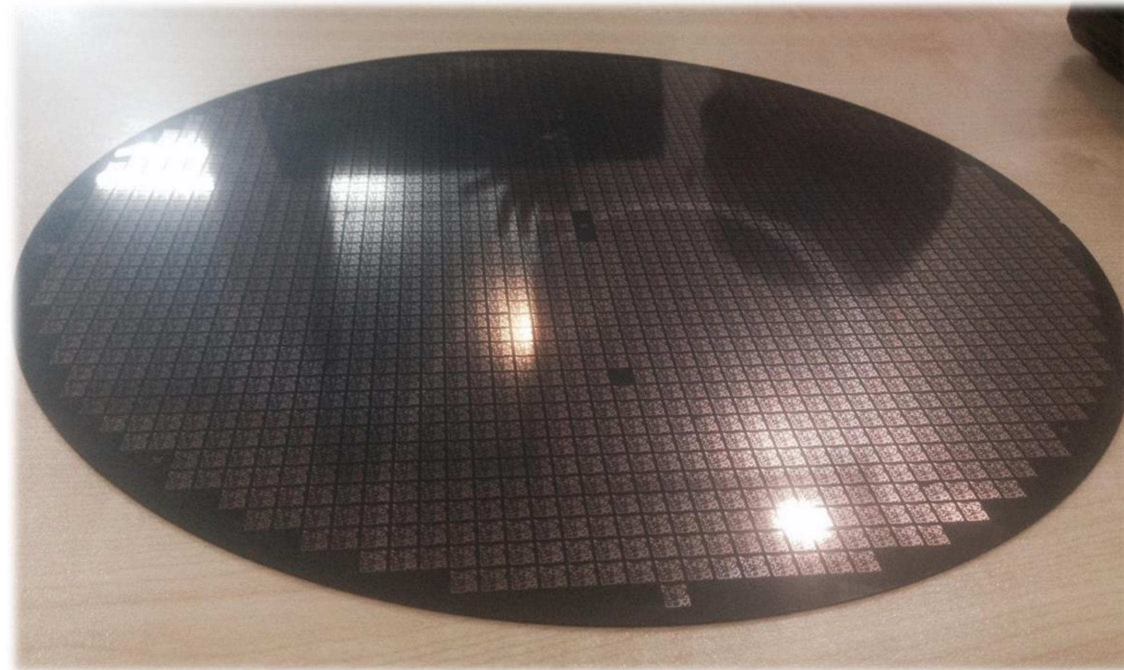
- Precision of monolithic silicon is lost - semiconductor devices are singulated & recombined in a physically different format to re-create a 300mm wafer (in plastic)
- Two major sources of positional variation





M-Series™ Basic Process Flow



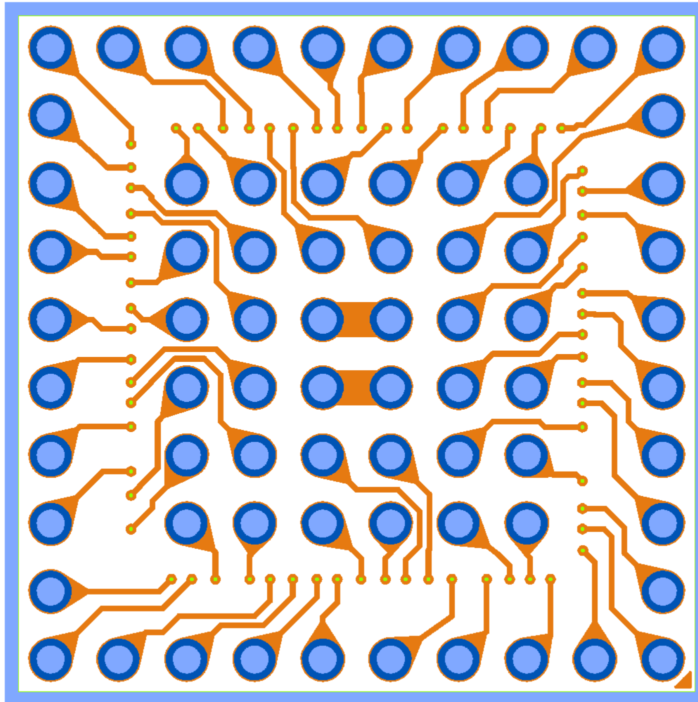


300mm plastic wafer (panel) post planarization

Adaptive Patterning™

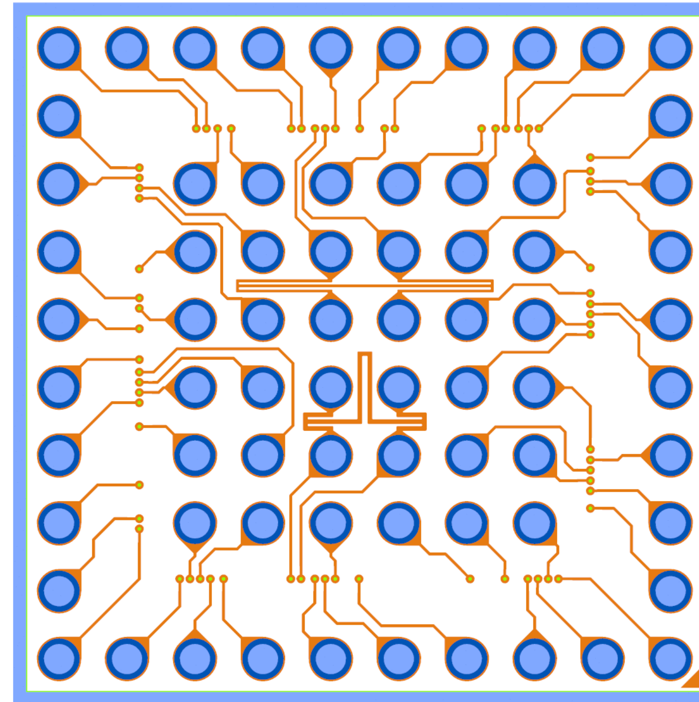
Adaptive Alignment

Align the entire RDL pattern to the measured die position

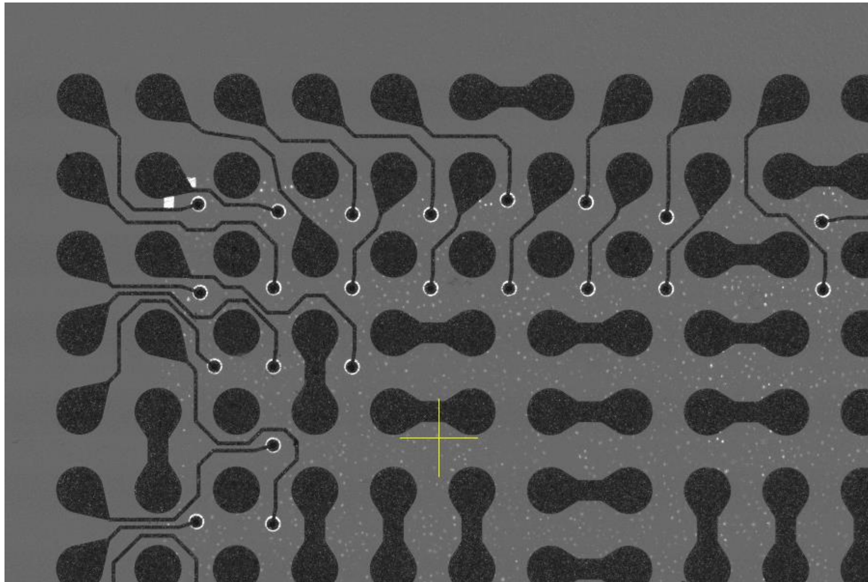


Adaptive Routing

Dynamically adapt RDL routing to the measured die position



Adaptive Patterning™ Example



- 6x6 mm die
- 8x8mm package
- Radial shift limit
- = 42.5µm
- Die shift yield
- = 100%

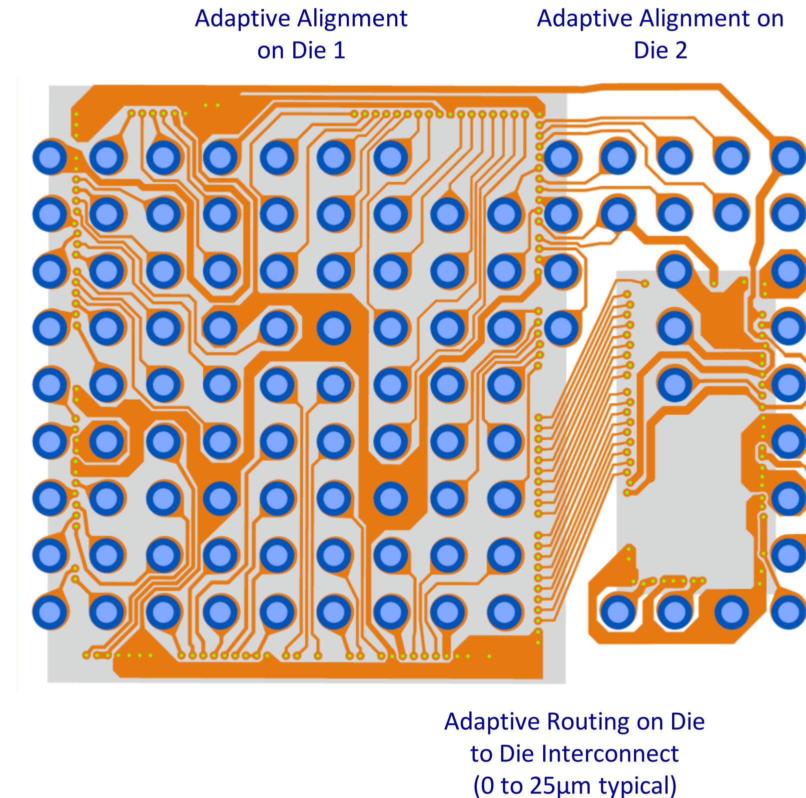
RF Application Example Detail

Multi-mode Adaptive Patterning™

Precise fixed RDL pattern alignment for both devices

100% routing yield for multi-die interconnect

Roadmap for differential pair matching



Scale of Adaptive Patterning

LSST - Large Synoptic Survey Telescope

- World's largest camera, 8.4m primary mirror
- Coming online in 2022 in Chile
- Maps the entire sky every two nights

LSST Camera Specs:

- 3.2 Gigapixels every 20 seconds
- 160 Megapixels per second

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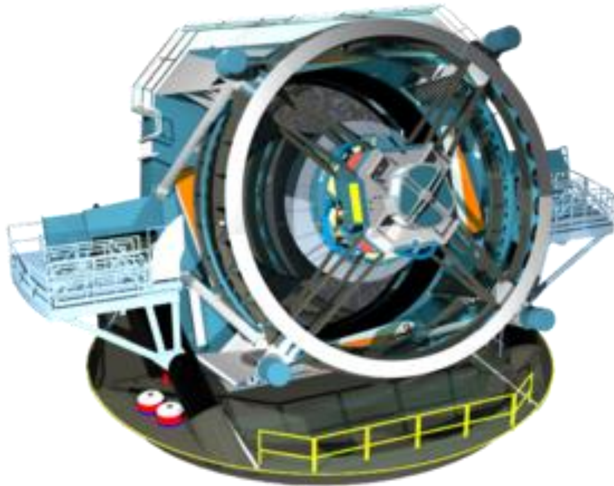

LSST Camera Specs:

- 3.2 Gigapixels every 20 seconds
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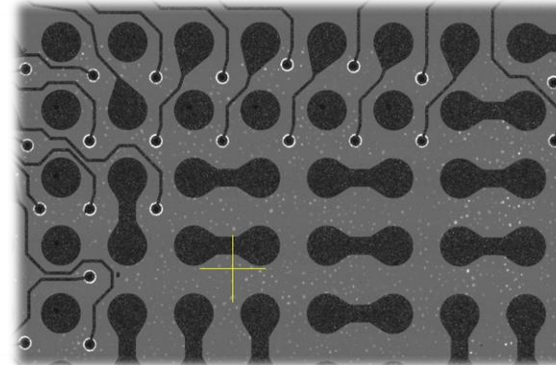
Deca's Adaptive Patterning

- 1st real-time design in manufacturing
- In production since 2018
- 300mm round reticle in single GDS II file

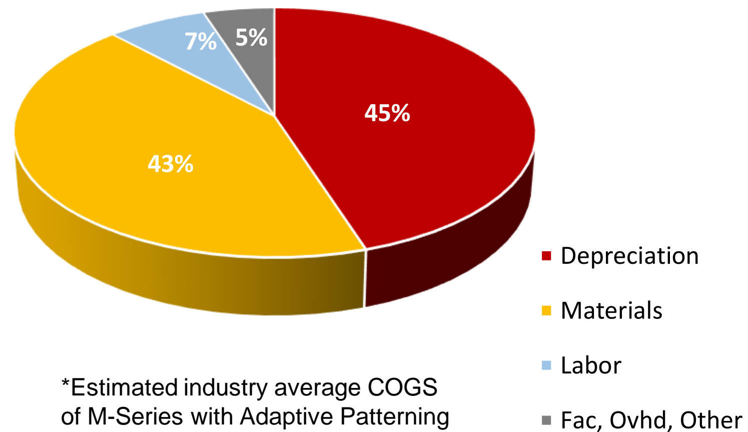


Adaptive Patterning Specs:

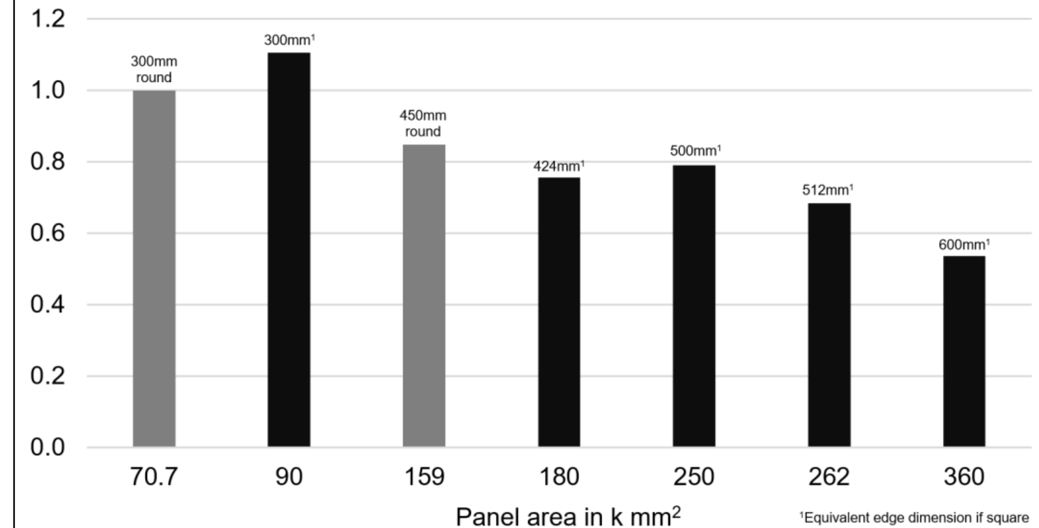
- 300mm designed & exposed each 28 seconds
- 90 Gigapixel file, 3.2 Gigapixels per second
- 600mm next gen 2µm system
  - 36 Terapixels in 140 seconds
  - 257 Gigapixels per second

Wafer Level Autoline – Via Cell

Why Large Panel M-Series



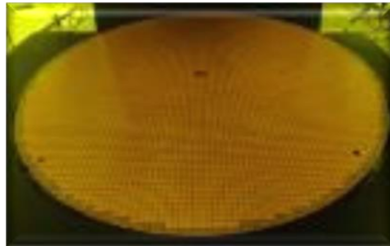
*Estimated industry average COGS of M-Series with Adaptive Patterning



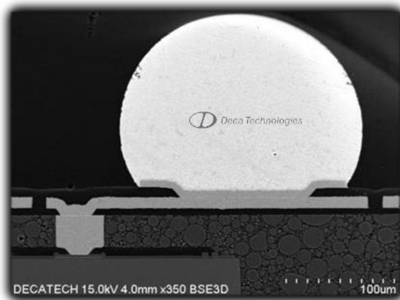
Scaling to Large Panel

… in cooperation with ASE

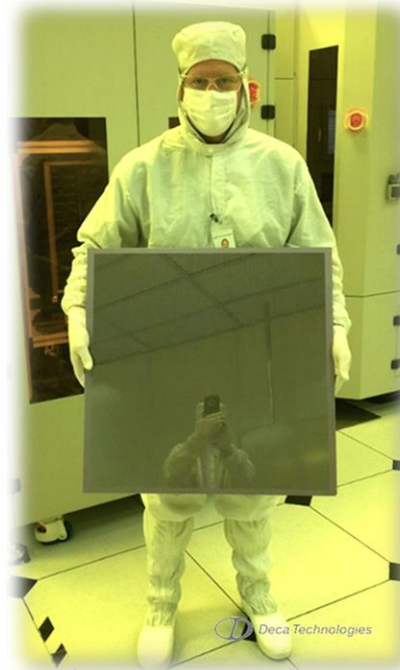
Initial Production



300mm round



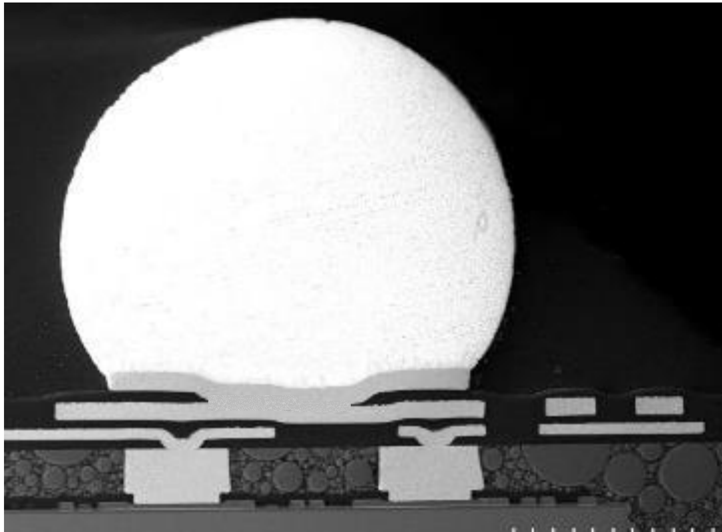
600mm Future Production



(post chip attach)

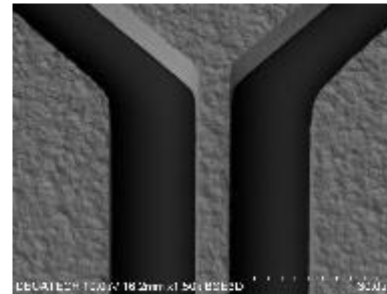
(post mold & debond)

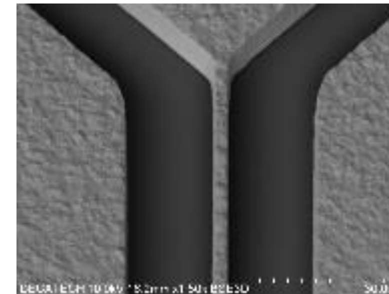
M-Series Building Blocks

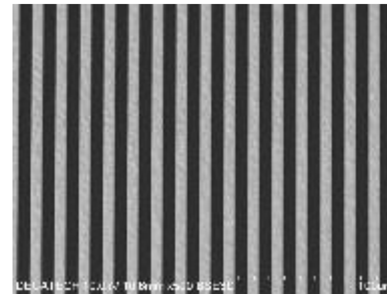

Multi-Layer, Multi-Thickness RDL & Dielectrics

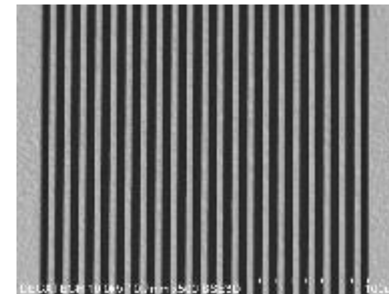
Direct Connect Cu Stud
Low contact resistance,
multi-via capture

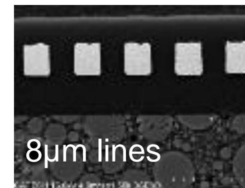
Polymer Isolated Via
CPI stress isolation,
tighter design rules

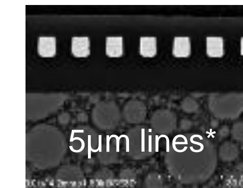

8µm Isolated Line


5µm Isolated Line*


8µm Nested Lines


5µm Nested Lines*





*Note: 5µm not yet released for production

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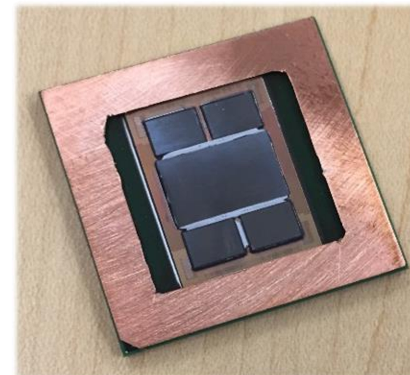
Heterogeneous SoC

Enabling cost-effect 2.5D with M-Series

- Silicon interposer replacement
- 2µm line & space, roadmap to 0.8µm
- 3 layer RDL, roadmap to 4 layers
- No reticle size limitations
  - 300mm round GDS II file (whole wafer)
  - 600mm square GDS II file (whole panel)
- Very low CPI risk (low-k dielectrics protected from flip chip reflow stress)
- High power dissipation path possible

Key initial applications

- Next generation mobile AP + memory
- Split die for yield enhancement (GPU, CPU)
- HBM to processor integration



M-Series as Si Interposer replacement SoC + HBM

M-Series as PCB replacement SoC + SerDes

Validation - Additional Investors in 2016

$60 million equity investment Jul'16

Signed TTLA (Technology Transfer & License Agreement)

- M-Series, Adaptive Patterning™ & Autoline
- Up-front NREs and ongoing royalties over 10 year term

Strong knowledge & experience base supporting Deca's success

$50 million equity investment Jul'16

Signed multi-year supply agreement

M-Series targeted on multiple mobile device applications

Wrapping Up

- Heterogeneous integration forms the track of the future for SoCs
- M-Series™ fan-out structure provides an ideal integration platform
- Adaptive Patterning™ (AP) enables high yield while scaling to fine pitch
- Elimination of stepper reticles with AP removes barriers to very large scale integration (80mm x 80mm test chip in process)
- Ability to scale from 300mm round to 600mm square creates breakthrough cost

However……

- The technical capabilities are progressing rapidly

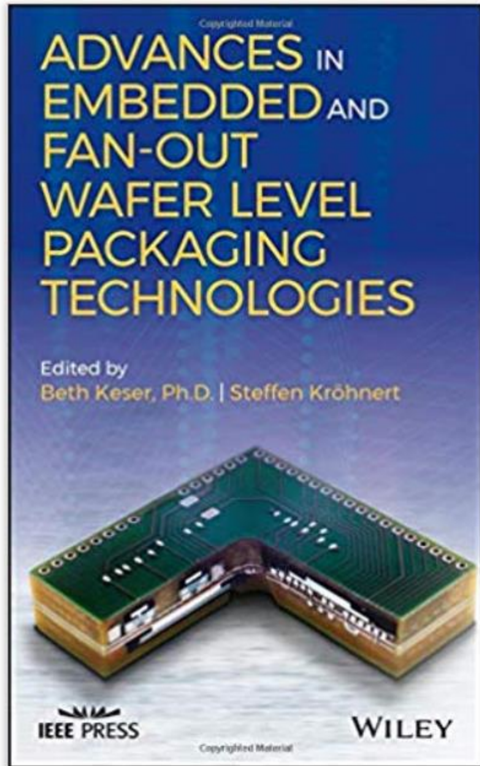
However……

- The technical capabilities are progressing rapidly

- But what about the supply chain ?
- So many unanswered questions….risk, liability, ownership etc.etc.
- How do we eliminate (or reduce) margin stacking to meet the cost targets ?
- Failure to do so will limit the heterogeneous integration implementation

#1 New Release in Computer Programming Logic

Look inside



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